GUJARAT TECHNOLOGICAL UNIVERSITY (GTU)

Competency-focused Outcome-based Green Curriculum-2021 (COGC-2021)
Semester-V

Course Title: VLSI Technology
(Course Code: 4353206)

Diploma programmer in which this course is offered	Semester in which offered
VLSI Technology	Vth

1. RATIONALE: This course will provide an opportunity to the ICT students to learn about fundamentals of VLSI Technology such as trends in VLSI, MOSFET structure and Analysis of MOS circuits. In laboratory part of this course, students will be given exposure to develop RTL code for different types of digital circuits. This subject is very important for the students for their carrier advancement in VLSI field.

2. COMPETENCY

The course content should be taught and implemented with the aim to develop required skills in the students so that they are able to acquire following competency:

- Circuit design using MOS transistors
- Develop and test Verilog programs for VLSI based electronic circuits.

3. COURSE OUTCOMES (COs)

1. Describe various VLSI design style, Design methodology, Design flow.
2. Understand structure and working of MOSFET and Scaling.
3. Understand characteristics of MOS inverter circuits for different load.
4. Design of combinational and sequential circuits using MOSFET.
5. Develop Verilog code for combinational and sequential design.

4. TEACHING AND EXAMINATION SCHEME

Teaching Scheme (In Hours)			Total Credits (L+T+P/2)	Examination Scheme				
				Theory Marks		Practical Marks		Total Marks
L	T	P	C	CA	ESE	CA	ESE	
3	0	2	4	70	30*	25	25	150

(*):Out of 30 marks under the theory CA, 10 marks are for assessment of the micro-project to facilitate integration of COs and the remaining 20 marks is the average of 2 tests to be taken during the semester for assessing the attainment of the cognitive domain UOs required for the attainment of the COs. Legends: L-Lecture; T – Tutorial/Teacher Guided Theory Practice; P -Practical; C – Credit, CA - Continuous Assessment; ESE -End Semester Examination.

5. SUGGESTED PRACTICAL EXERCISES: NA

The following practical outcomes (PrOs) are the subcomponents of the Course Outcomes (Cos). Some of the PrOs marked '*' are compulsory, as they are crucial for that particular CO at the 'Precision Level' of Dave's Taxonomy related to 'Psychomotor Domain'.

Sr. No.	Practical Outcomes (PrOs)	Unit No.	Approx. Hrs. Required
1.	Identify Verilog modules and coding styles in Verilog	**V**	**2**
2.	Simulate the Basic logic gates using Verilog	**IV, V**	**2**
3.	Simulate universal gates using Verilog	**IV, V**	**2**
4.	Simulate XOR and XNOR using Verilog	**IV, V**	**2**
5.	Simulate Half adder using Verilog	**IV, V**	**2**
6.	Simulate full adder using half adder in Verilog	**IV, V**	**2**
7.	Simulate four bit adder using Verilog	**IV, V**	**2**
8.	Simulate 4 x1 multiplexer using Verilog	**IV, V**	**2**
9.	Simulate 1 x 4 de-mux using Verilog	**IV, V**	**2**
10	Simulate 3 : 8 decoder using Verilog	**IV, V**	**2**
11	Simulate 8 : 3 encoder using Verilog	**IV, V**	**2**
12	Simulate Parity generator and checker using Verilog	**IV, V**	**2**
13	Simulate flip-flops (SR , D, T, JK) using Verilog	**IV, V**	**2**
14	Simulate 4 bit Up counter using Verilog	**IV, V**	**2**
15	Simulate 4 bit shift register using Verilog	**IV, V**	**2**
16	Verify digital circuits by implementing testbench for it inVerilog	**IV, V**	**2**
17	Hardware implementation of above programs	**I, IV,V**	**2**
			28 Hrs

(a) More Practical Exercises can be designed and offered by the respective course teacher to develop the industry relevant skills/outcomes to match the COs. The above table is only a suggestive list.

(b) perform any of the practical exercises for a total of minimum 28 hours from above list depending upon the availability of resources so that skills matching with the most of the outcomes in the every unit is included

6. MAJOR EQUIPMENT/ INSTRUMENTS REQUIRED

Sr.No.	Equipment Name with Broad Specifications	PrO. No.
1	Computer System	ALL
2	Verilog Simulator Software	ALL
3	VLSI Trainer Kits	ALL

Software/Learning Websites

I. ISE Simulator
II. QUARTUS-II-ALTERA EVAL VERSION
III. Modalism® HDL simulator for use by students in their academic coursework.
IV. ISE Simulator
V. https://www.edaplayground.com/
VI. https://vlab.amrita.edu/?sub=3&brch=66&sim=532&cnt=867

7. AFFECTIVE DOMAIN OUTCOMES:

The following ***sample*** Affective Domain Outcomes (ADOs) are embedded in many of the above-mentioned COs and PrOs. More could be added to fulfill the development of this competency.

1. Work as a leader/a team member.
2. Follow ethical practices.

8. UNDERPINNING THEORY:

Only the major Underpinning Theory is formulated as higher level UOs of *Revised Bloom's taxonomy* in order development of the COs and competency is not missed out by the students and teachers. If required, more such higher level UOs could be included by the course teacher to focuson attainment of COs and competency.

Unit	Unit Outcomes (UOs) (4 to 6 UOs at Application and above level)		Topics and Sub-topics
Unit – I. Introductio n to VLSI	**1a**	Describe Overview of VLSI Design Methodologies, VLSI design flow	1.1 VLSI design Methodology, Time to Market, Major Constraints for chip designing, ASIC Design flow 1.2 Y-Chart
	1b	Explain Design Hierarchy, Concept of Regularity, Modularity and Locality,	1.3 Concept of Top-Down, Bottom-Up approach 1.4 regularity, modularity, locality

	1c	Explain VLSI Design styles: Full Custom, Semi-Custom	1.5 Overview of FPGA, Gate Array Design, Standard Cell Based Design, Full Custom Design
Unit– II MOS Transistor	**2a**	Explain MOSFET structure and its working under different bias conditions.	1.6 Explain Energy band Diagram and Structure of MOS 1.7 The MOS System under External Bias
	2b	Explain Operation of MOS Transistor (MOSFET) and voltage- current characteristics	2.1 Channel formation 2.2 Symbols for different MOSFET 2.3 MOSFET Current-Voltage characteristics 2.4 Gradual channel Approximation
	2c	Explain MOSFET Scaling	2.5 Needs of scaling 2.6 Full-Voltage Scaling, Constant-Voltage Scaling. 2.7 Effect of Scaling
Unit– III MOS Inverters	**3a**	Describe Basics of MOSFET inverter	3.1 Concept and working of Ideal Inverter 3.2 Noise Margin 3.3Voltage Transfer Characteristics
	3b	Describe Resistive load Inverter	3.4 Working and VTC without derivation
	3c	Differentiate Inverter with n-type MOSFET load (Enhancement & Depletion type MOSFET load),	3.5 Working and VTC without derivation for Enhancement & Depletion type MOSFET load
	3d	Explain CMOS Inverter and its characteristics	3.6 Working and VTC without derivation for CMOS inverter
Unit– IV MOS Circuits	**4a**	Explain two input NAND and NOR Gate with depletion NMOS load.	4.1 MOS logic circuits with Depletion nMOS Loads
	4b	Explain Two input NAND and NOR Gate using CMOS logic.	4.2 CMOS logic circuits ,Stick Diagram, Euler path Approach

	4c	Differentiate AOI and OAI Logic. Design simple XOR function	4.3 Complex logic circuits
	4d	Describe the working of SR latch circuit. Distinguish Clocked latch and Flip-Flop circuit	4.4 The SR latch circuit, 4.5 Clocked latch and Flip-flop circuit 4.6 CMOS D-latch and Edge-triggered flip-flop
Unit– V Verilog Programming	**5a**	Describe Verilog: HDL fundamentals, simulation, coding style and test-bench design	7.1 Module definition 7.2 RTL coding style: Gate level, Data flow, Behavioral, Mixed approach 7.3 Stimulus generation
	5b	Develop Verilog Programs related to basic logic gates	5.4 Basic Logic gate implementation in Verilog
	5c	Develop Verilog Programs related to Fundamental Arithmetic operations.	5.5 Verilog code for adder and subtractor circuits
	5d	Develop Verilog Programs related to Combinational circuits.	5.6 Combinational circuits: Multiplexer , Demultiplexer, Decoder and Encoder, Parity Generator and parity checker.
	5e	Develop Verilog Programs related to Sequential circuits.	5.7 Basic Sequential circuits : SR latch, D F/F, T F/F, JK F/F 5.8 Parallel input Parallel output Shift Register, Up Counter, Down Counter

9. SUGGESTED SPECIFICATION TABLE FOR QUESTIONPAPER DESIGN:

Unit	Unit Title	Teaching Hours	Distribution of Theory Marks			
			R Level	U Level	A Level	Total Marks
1	Introduction to VLSI	**6**	2	6	6	**10**
2	MOS Transistor	**8**	4	8	2	**14**
3	MOS Inverters	**6**	5	5	2	**12**
4	MOS Circuits	**10**	2	6	10	**18**

5	Verilog Programming	**12**	2	2	12	**16**
Total		**42**	**18**	**22**	**30**	**70**

10. SUGGESTED STUDENT ACTIVITIES:

Other than the laboratory learning, following are the suggested student-related ***co-curricular*** activities which can be undertaken to accelerate the attainment of the various outcomes in this course: Students should conduct following activities in group and prepare reports of each activity.

- Prepare chart to represent the CMOS design process
- Prepare chart to represent the technological advancements in CMOS technology starting fromtransistors to current technology
- Project- Build a small ASIC for your Home /Community.
- Prepare chart showing the types of FPGA technology
- List out methods used in industries for each step used in CMOS design process.

These are sample strategies, which the teacher can use to accelerate the attainment of the variousoutcomes in this course:

i. Show Video/ Animation film explaining VLSI Design which are available on internet.
ii. Arrange expert lecture on VHDL programming for real life applications.
iii. Massive open online courses (MOOCs) may be used to teach various topics/sub topics.
iv. Guide students for using latest Technical Magazine
v. Visit industries where equipment/gadgets using VLSI are being manufactured/ assembled.
vii. Guide student(s) in undertaking micro-projects.

11. SUGGESTED SPECIAL INSTRUCTIONAL STRATEGIES (if any)

Only one micro-project is planned to be undertaken by a student that needs to be assigned to him/her in the beginning of the semester. In the first four semesters, the micro-project is group- based. However, in the fifth and sixth semesters, it should be preferably be ***individually*** undertaken to build up the skill and confidence in every student to become problem solver so thats/he contributes to the projects of the industry. In special situations where groups have to be formed for micro-projects, the number of students in the group should ***not exceed three.***

The micro-project could be industry application based, internet-based, workshop-based, laboratory-based or field-based. Each micro-project should encompass two or more COs which arein fact, an integration of PrOs, UOs and ADOs. Each student will have to maintain dated work diary consisting of individual contribution in the project work and give a seminar presentation of it before submission. The total duration of the micro-project should not be less than ***16 (sixteen) student engagement hours*** during the course. The student ought to submit micro-project by the end of the semester to develop the industry-oriented COs.

A suggestive list of micro-projects is given here. This has to match the competency and the COs.Similar micro-projects could be added by the concerned course teacher.

12. SUGGESTED PROJECT LIST:

MICRO PROJECT 1: Prepare following Items.

1. Prepare graph showing relationship between feature size, number of transistors and year (Silicon Roadmap).
2. Prepare graph showing various design methodology.

MICRO PROJECT 2: Design Application oriented basic Project using FPGA.

1. Design and Implement LED flasher circuit.
2. Design and Implement circuit for relay-based operation using switch.
3. Design and Implement Room Temperature Monitor/Controller System.
4. Design and Implement Water Level Indicator/controller circuit

MICRO PROJECT 3: Prepare following Items.

1. Prepare chart indicating the types of etching processes used with its application.
2. Prepare chart indicating the deposition processes with its application.
3. Prepare a survey report on the types of transistors used in memory elements.
4. Prepare a survey report on requirements of clean room and its classification

13. SUGGESTED LEARNING RESOURCES:

Sr. No.	Title of Book	Author	Publication
1.	CMOS DIGITAL INTEGRATED CIRCUITS	Sung Mo Kang	TMH
2.	Introduction to VLSI Circuits and Systems.	Uyemura J.P.	WILEY INDIA PVT. LTD.
3.	VLSI DESIGN	Das Debaprasad	OXFORD
4.	VLSI DESIGN Theory and Practice	Vij Vikrant, Er. Syal Nidhi	LAXMI PUBLICATIONS PVT. LTD.
5.	CMOS Circuit Design, Layout, and Simulation	Baker, Li, Boyce	Wiley
6.	Verilog HDL : A Guide to Digital design and Synthesis	Samir Palnitkar	SunSoft Press
7.	A Verilog HDL Primer.	Bhasker (J).	Bsp ProfessionalBooks

14. SOFTWARE/LEARNING WEBSITES

1 https://eda.sw.siemens.com/en-US/
2. https://nptel.ac.in/courses/117106092
3. https://nptel.ac.in/courses/103106075
4. https://archive.nptel.ac.in/courses/113/106/113106062/

15. PO-COMPETENCY-CO MAPPING:

Program Outcomes (POs):

Basic & Discipline specific knowledge: An apply knowledge of basic mathematics, scienceand engineering fundamentals and engineering specialization to solve the engineering problems.
Problem Analysis: Identify and analyze well defined engineering problems using codifiedstandard methods.
Design/ Development of Solution: Design solutions for well-defined technical problems andassist with the design of systems, components or processes to meet specified needs.
Engineering Tools, Experimentation and Testing: Apply modern engineering tools andrelevant technique to conduct standard tests and measurements.
Engineering practices for Society, Environment and sustainability: Apply relevanttechnology in context of Society, sustainability, environment and ethical practices.
Project Management: Use engineering management principles individually, as a team memberor a leader to manage projects and effectively communicate about welldefined engineering activities.
Life-long learning: Ability to analyze individual needs and engage in updating in the context ofcontext of technological changes.

Semester V	**Biomedical Engineering Project-I (Course Code:4350304)**						
	POs						
Competency & Course Outcomes	**PO 1 Basic & Discipline specific knowledge**	**PO 2 Problem Analysis**	**PO 3 Design/ develop-ment of solutions**	**PO 4 Engineering Tools, Experimen-tation & Testing**	**PO 5 Engineering practices for society, sustainability & environment**	**PO 6 Project Manage-ment**	**PO 7 Life-long learning**
Competency	**Maintain various types of A.C. machines and three -phase transformers safely.**						
Course Outcomes CO1 Describe various VLSI design style, Design methodology, Design flow.	3	2	2	3	2	3	3
CO2 Understand structure and working of MOSFET,	3	3	2	1	1	2	3

MOSFET Geometry Scaling.							
CO3 Understand the working and characteristics of MOS inverter circuits for different load.	3	2	3	2	2	2	3
CO4 Design of combinational and sequential circuits using MOSFET.	3	3	3	2	2	2	2
CO5 Develop Verilog code for combinational and sequential design	2	3	3	3	3	3	2

*Legend: '**3'** for high, '**2**' for medium, **'1'** for low and **'-'** for no correlation of each CO with PO.*

16. COURSE CURRICULUM DEVELOPMENT COMMITTEE

GTU Resource Persons

Sr. No.	Name and Designation	Institute	Contact No.	Email
1.	GIREEJA DINESHCHANDRA AMIN	GGP, AHMEDADAD	7574850311	gireeja.amin@gmail.com